CASE NO. 5050/713

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:)
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Joseph Urbano et al.) Group Art Unit: 3737
)
Serial No.: 09/396,486) Examiner: F. Jaworski
)
Filed: September 14, 1999)
)
For: MEDICAL DIAGNOSTIC ULTRASOUND SYSTEM)
AND METHOD)

DECLARATION PURSUANT TO 37 C.F.R. 1.131

I hereby declare that:

1. I have reviewed the claims of the above referenced application and believe I am a joint inventor. I am listed as a joint inventor in the above referenced application.

2. Prior to June 8, 1998 in the United States of America, an ultrasound system using a scan converter was tested and operated. The scan converter included a single field programmable gate array (FPGA) that operated to interpolate data and generate memory addresses for the interpolation to convert data formatted in a polar coordinate system to a Cartesian coordinate format. Attached at Tab A is a copy of a photo of a digital board prototype that was tested and operated prior to June 8, 1998. The identification bubbles have been more recently added. The block diagram at Tab A shows the tested ultrasound system and use of FPGA's, including one FPGA for the scan converter. The block diagram was created after June 8, 1998 to represent the digital board prototype as it existed prior to June 8, 1998. Other devices in the scan converter included memories and a formatter FPGA that prepares incoming data for scan conversion by the FPGA. The scan converter FPGA performs substantially all of the coordinate conversion function of the scan conversion, including interpolation and generation of memory addresses. Attached at Tab B are (1) a Final Project Report and (2) Minutes of Board of Directors Meeting, both from prior to June 8, 1998, indicating operation of the prototype digital board.

3. As further evidence, attached at Tab C is an invoice showing delivery of the backend board (the digital board pictured at Tab A) that included the scan converter FPGA described above. A second invoice shows delivery of the analog board for connecting with the backend board. Both deliveries occurred prior to June 8, 1998.

4. An FPGA was used in multiple subsystems of the tested ultrasound system, including the

scan converter as discussed above, a transmit beamformer and a receive beamformer (See the block diagram attached at Tab A). FPGAs used in the transmit beamformer on the Analog Board generated digital transmit waveforms from memory samples. FPGAs used in the receive beamformer on the digital board applied relative delays and summed samples from 64 elements of a linear transducer. In response to a change in mode, the FPGAs of the beamformers or scan converter were re-programmed. By June 8, 1998, a further system was tested and operated. This further system was under 30 pounds and designed to be portable or carried by a user.

5. After reducing to practice the ultrasound system described above, further refinements, functionality, testing and development work continued until the commercial introduction of the Acuson Cypress system.

6. All statements herein made of my own knowledge are true and all statements herein made on information and belief are believed to be true. I acknowledge that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon.

11/27/01

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